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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/080,568	02/25/2002	Stephen M. Gates	YOR919980324 US2	9141

21254 7590 08/18/2003  
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EXAMINER

CAO, PHAT X

ART UNIT	PAPER NUMBER
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2814

DATE MAILED: 08/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/080,568

Applicant(s)

GATES ET AL.

Examiner

Phat X. Cao

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 27 June 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 11-18 and 26-35 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 11-18 and 26-35 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 10.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

### **DETAILED ACTION**

1. The Request for Continued Examination filed 6/27/03 in Paper No. 9 is acknowledged.

#### ***Claim Rejections - 35 USC § 112***

2. Claim 11 recites the limitation "said metal conductor" in line 14. There is insufficient antecedent basis for this limitation in the claim.
3. Claim 32 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 32 depends on base claim 26. The base claim 26 is disclosed a semiconductor device structure of Fig. 5B or Fig. 6B. However, none of Figs. 5B and 6B disclose the semiconductor node forming a part of a field effect transistor. Therefore, the limitation "..., each node in said plurality of semiconductor nodes forming a part of each field effect transistor (claim 32)" is not supported by the original disclosure.

#### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 11-12, 15-16, 18, 26, 28-29, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Durlam et al (US. 5,940,319).

With respect to claims 11-12, 18, 26, 28-29 and 33, Durlam's first embodiment (Figs. 5-8) discloses an array of microelectronic elements comprising: a substrate of semiconductor material 11; a lower layer of dielectric material (12a,21,25) disposed with a lower surface in contact with the substrate and an upper surface in spaced adjacency thereto; a pattern of mutually electrically isolated conducting regions (19a,37) and (19b,38) (Fig. 5) disposed within the lower layer of dielectric material, the conducting regions extending to the upper surface of the lower layer, an upper layer of dielectric material 51 disposed with a lower surface thereof in contact with and bonded to the upper surface of the lower layer; and a plurality of nodes of MTJs 43 and 44 disposed within the upper layer of dielectric material, each of the nodes being in electrical contact with only one of the conducting regions at the upper surface of the lower layer, wherein each conducting region comprises: a via 37 formed on a metal conductor 19a and comprising a diffusion barrier material of Ta (not illustrated, see column 3, lines 35-42) which electrically contacts a node 43 in the plurality of nodes and electrically connects the metal conductor 19a with the node 43.

Durlam's first embodiment does not disclose the plurality of nodes including semiconductor diodes.

However, Durlam further teaches a second embodiment of MRAM (Fig. 17)

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having a plurality of nodes which include diodes 93 and 95 in contact with the conducting regions 82 at the upper surface of the lower layer. Accordingly, it would have been obvious to modify the first embodiment by forming the plurality of nodes with the structure as suggested by the second embodiment for the purpose of switching a magnetic memory element to read information in the magnetic memory element (column 6, lines 26-30).

With respect to claims 15-16, Durlam (Fig. 8) further discloses that the device comprises a field effect transistor 12a, a first insulating layer 54 is disposed over an upper surface of the upper layer, and a second insulating layer 33 is formed over the upper surface of the lower layer.

6. Claims 13-14, 17, 27 and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Durlam et al in view of Bronner et al (US. 6,242,770).

Durlam does not disclose that diodes are single crystal Si diodes.

However, it would have been obvious to form Durlam's diodes as single crystal Si diodes because according to Bronner, such single crystal Si diodes (column 9, lines 63-65) would provide high conductivity, high rectification and low total resistance (column 3, lines 1-4).

7. Claims 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Durlam et al in view of Oda (US. 5,994,749).

Durlam's first embodiment (**Figs. 5-8**) does not specifically disclose the metal conductor 19a being formed of a different material than the via 37.

However, Oda (Fig. 5) teaches the forming of a conventional conductive contact

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structure comprising an aluminum layer 114 in electrical contact with the via 118 made of tungsten (column 1, lines 28-36). Accordingly, it would have been obvious to form the metal conductor 19a and the via 37 of Durlam with the materials as set forth above because as taught by Oda, such materials are well known materials which are used for the wirings in a conductive contact structure.

### ***Response to Arguments***

8. Applicant argues that Durlam does not teach or suggest “a via formed on said metal conductor and comprising a diffusion barrier material which contacts a node in said plurality of nodes and electrically connects said metal conductor with said node”.

Applicant’s argument is not persuasive because Durlam clearly states at column 3, lines 38-42:

“In order to improve adhesion of field focusing layer 24 and to provide a barrier for Ni or Fe diffusion into the conductor and/or dielectric **a layer of Ta or TaN or such materials could be added between field focusing layer 24 and conductive layer 26.**” (fig. 3)

Therefore, Durlam does teach “a via [37] formed on said metal conductor [19a] and comprising a diffusion barrier material [not illustrated, see above statement] which [electrically] contacts a node [43] in said plurality of nodes and electrically connects said metal conductor [19a] with said node [43]”.

Applicant further argues that in Durlam’s Fig. 5, the conductive via 37 does not connect the metal conductor 19a to a “semiconductor” because the conductor layer 34 is not a “semiconductor”.

This argument is not persuasive because Durlam’s Fig. 5 is not relied on for teaching the conductive via connecting to a “semiconductor”, but rather, Durlam’s Fig.

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17 is relied on for showing the known feature of connecting the conductive via 82 to the "semiconductor" diode 93 for the purpose of switching a magnetic memory element to read information in the magnetic memory element (see ground of rejection for more details).

Applicant further argues that Durlam's Fig. 17 does not suggest a conductive via "comprising a diffusion barrier material which contacts a node" because the diodes 93 and 95 formed directly on the conductive via 82 will result an reaction between the semiconductor diodes and the conductive via.

It appears Applicant argues that the diffusion barrier material must be disposed between the conductive via and the semiconductor diodes for prevent the reaction between the semiconductor diodes and the conductive via. However, the limitation of having the diffusion barrier material disposed between the conductive via and the semiconductor node does not seem to be required by the claim language. Therefore, Applicant's argument is not persuasive because as previously discussed, Durlam does suggest a conductive via "comprising a diffusion barrier material which [electrically] contacts a node" as claimed because Durlam clearly states at column 3, lines 40-42 that "a layer of Ta or TaN or such material could be added between field focusing layer 24 [or 84] and conductor layer 26 [or 82]."

With respect to the combination of Durlam and Bronner, Applicant argues that "the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner."

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This is incorrect because in the last Office Action, the Examiner clearly points to motivation or suggestion in the references to urge the combination as alleged by the Examiner. Specifically, the Office Action states: "... because according to Bronner, such single crystal Si diodes (column 9, lines 63-65) would provide high conductivity, high rectification and low total resistance (column 3, lines 1-4)."

With respect to the combination of Durlam and Oda, Applicant argues that it is improper to combine Oda with Durlam because Oda teaches the tungsten plug 18 connecting an aluminum alloy wiring layer 14 to another aluminum alloy wiring layer 19, but not to a semiconductor node.

It should be noted that the rejection of claims 34-35 is not based on anticipation, but rather, is based on obviousness. In this case, Oda is not relied on for teaching a conductive region in contact with a semiconductor node. Durlam discloses a conductive region in contact with a semiconductor node. Oda is only relied on for showing that it was known to form a conductive region having a metal conductor being formed of a different material than the conductive via. The Examiner thus regards the Applicant's assertions as constituting evidence that the Applicant has failed to consider as a whole the prior art teachings disclosed by the combining of the references.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (703) 308-4917. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers

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for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

PC  
August 8, 2003

  
PHAT X. CAO  
PRIMARY EXAMINER